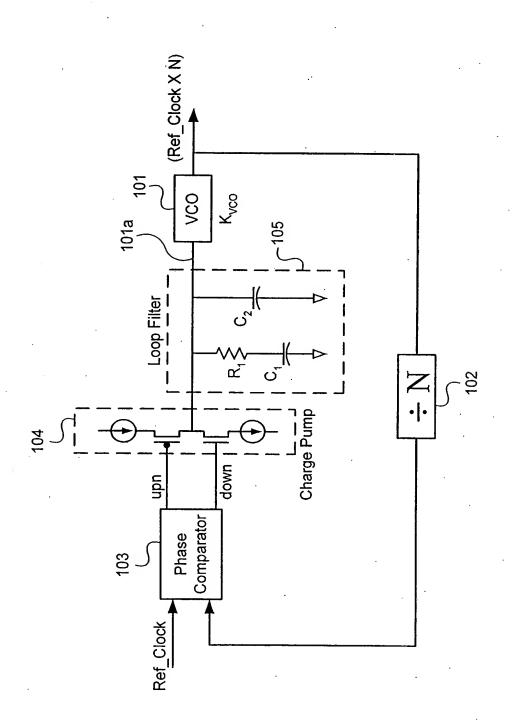
Express Mail No.: EV 442673922 US
Title: Method And Apparatus For Automatically
Generating A Phase Lock Loop (PLL)
Inventor(s): John Horan et al.
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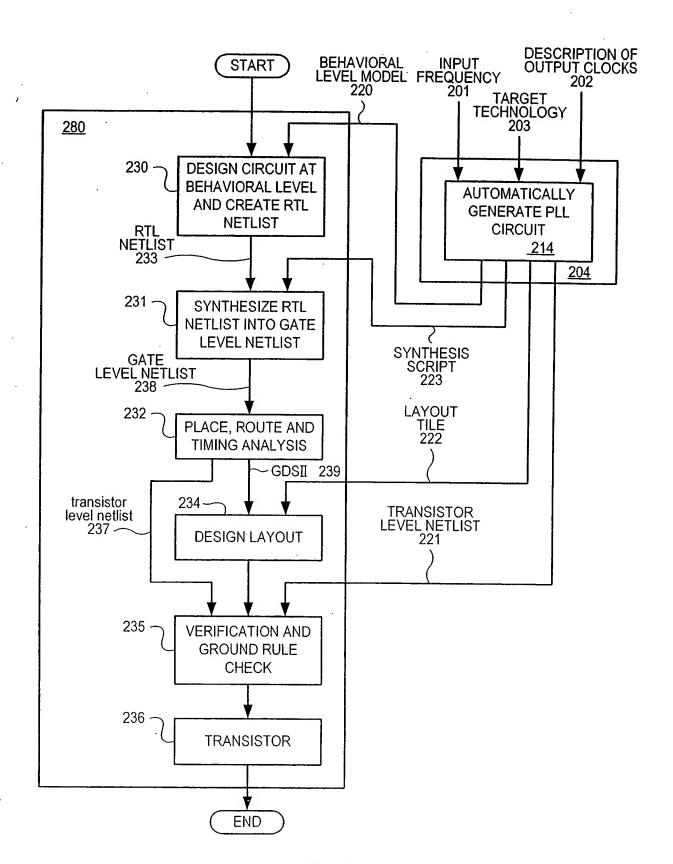


FIG. 2

Title: Method And Apparatus For Automatically Generating A Phase Lock Loop (PLL)

Inventor(s): John Horan et al.

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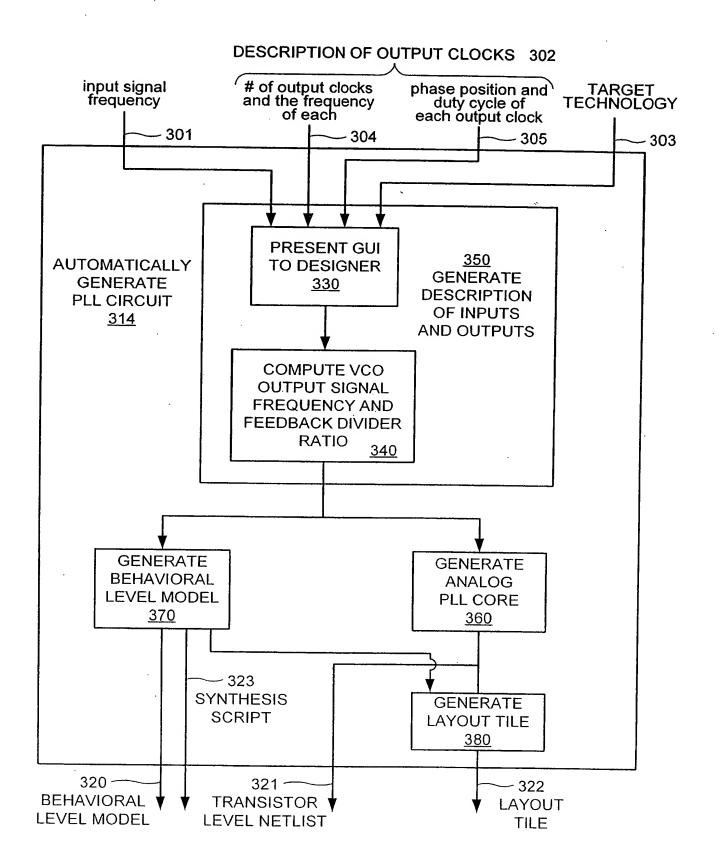
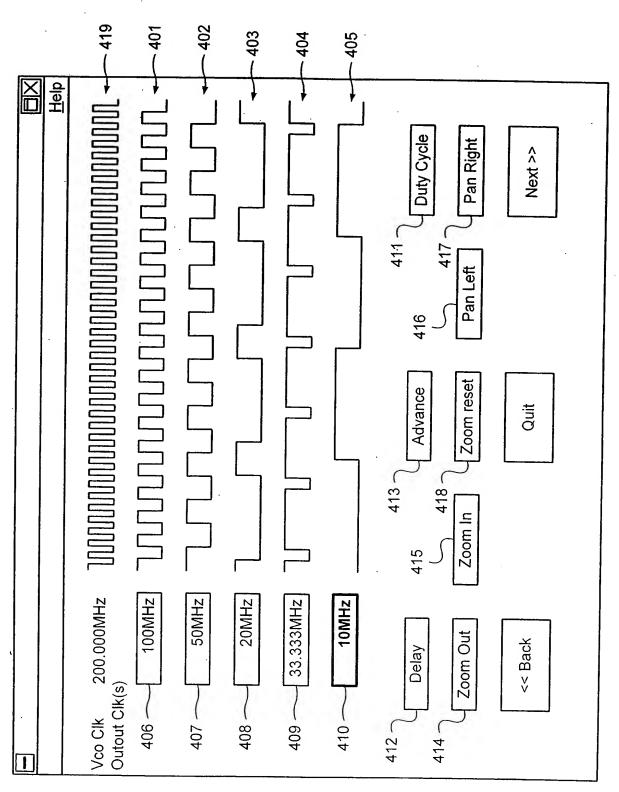


FIG. 3

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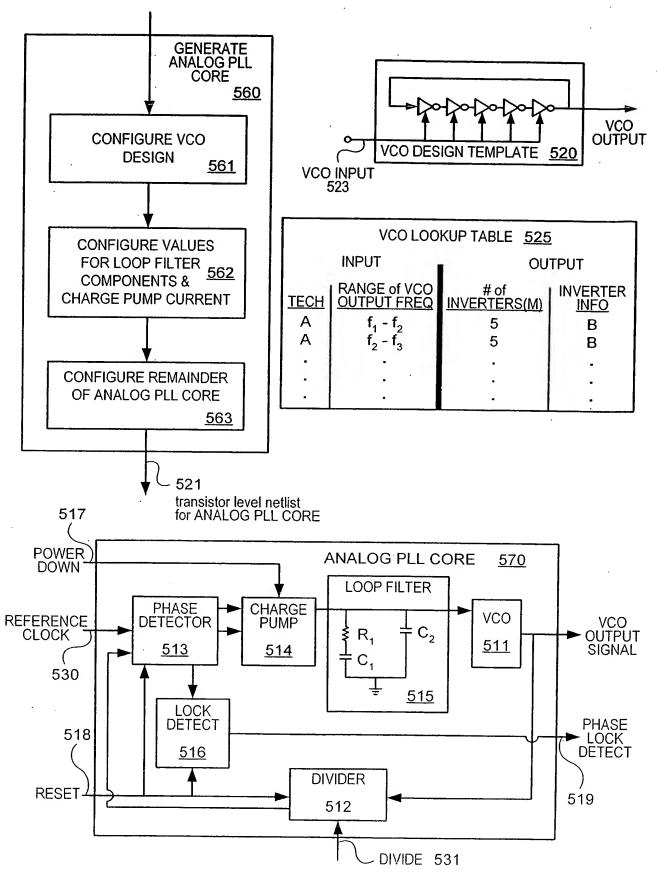


FIG. 5

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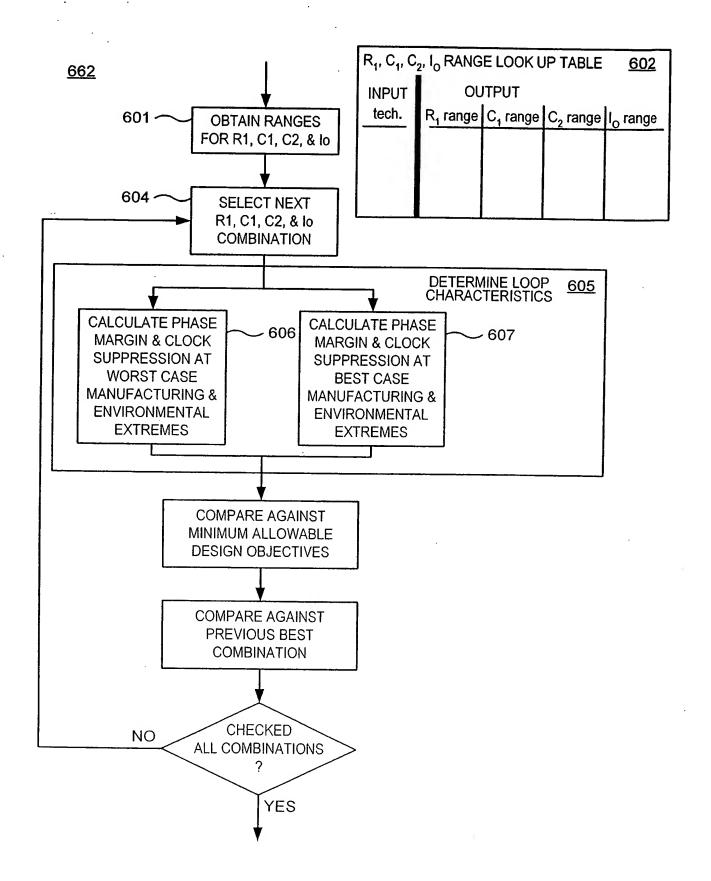
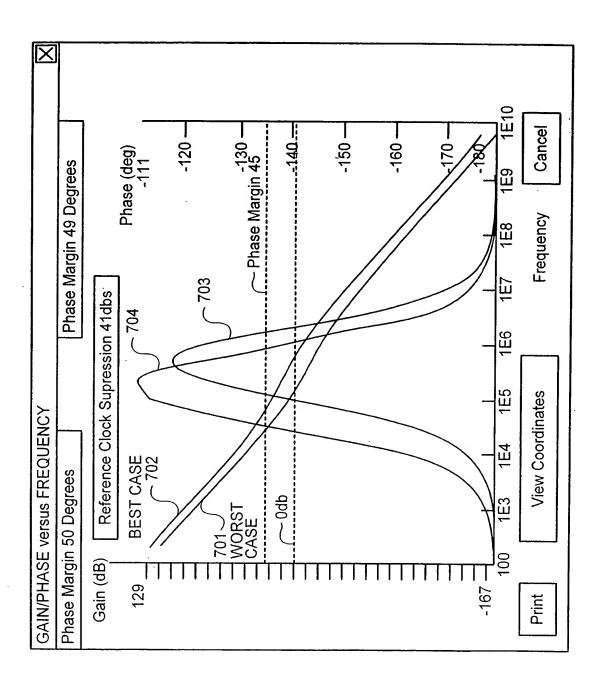


FIG. 6

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	fast PLL simulator				X
		System Parameters	ımeters		
801	Kvco [Mhz/V] 116.363	116.3636363	cp[pF]	150	
	R [KOhm] 20		cp[pF]	2	
	lcp [um] 9	<u>e</u>	In Freq [MHz]	10	
		Feedb	Feedback divider	8	
	Simulation Parameters	neters		☐ Initial Frequency error	
802	Filter leakage	1e-13	□ Initi	☐ Initial Phase Upset	
	Input Jitter Sigma [pS]	100		Simulate	
008	Num Cycles	100		Exit	
					7

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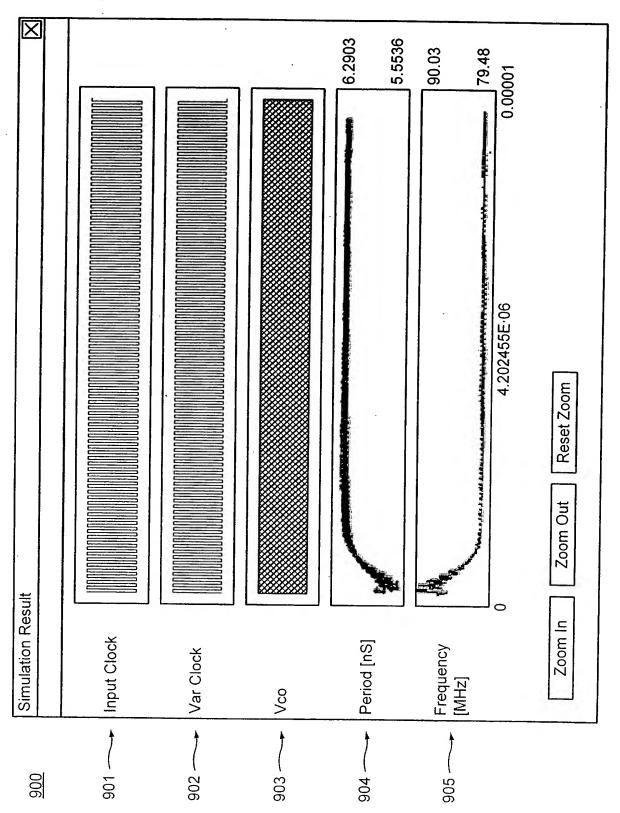


FIG. 9

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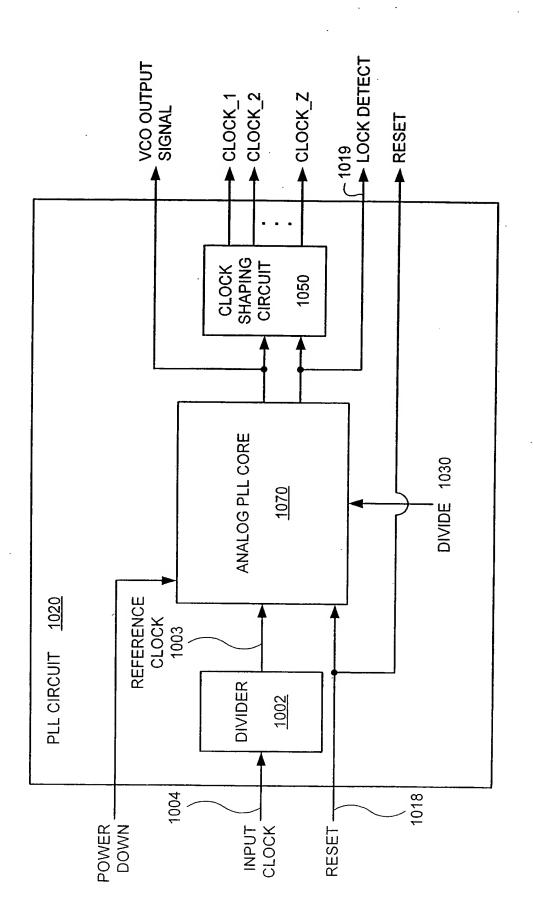


FIG. 10

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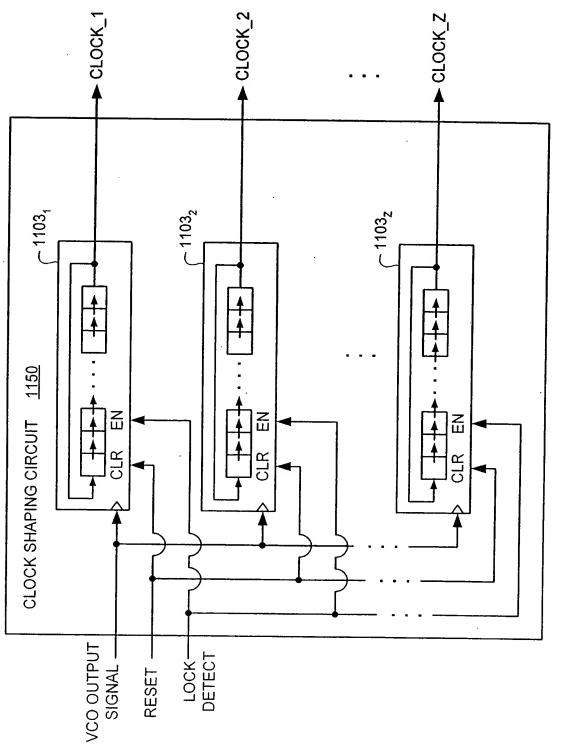


FIG. 11

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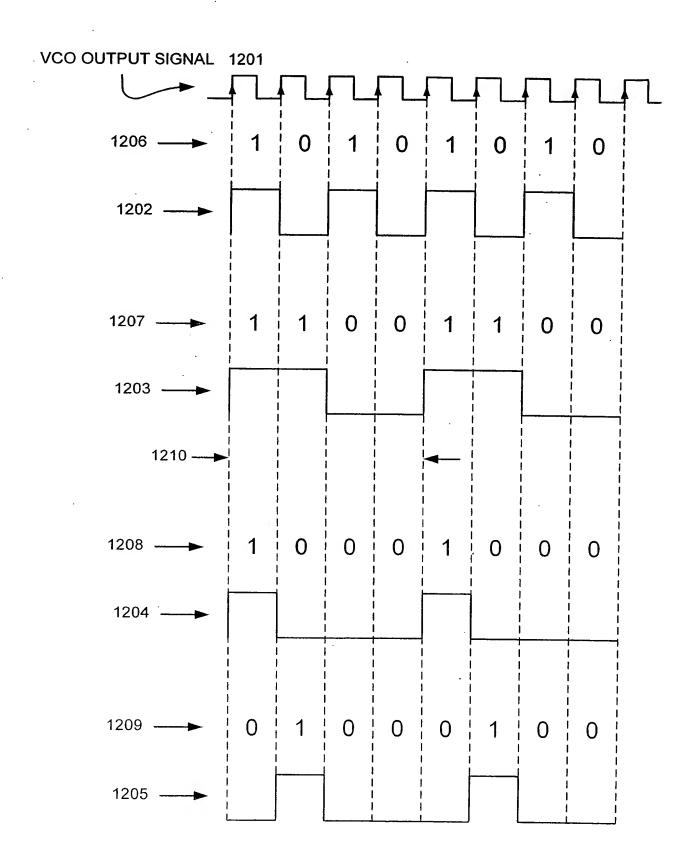


FIG. 12

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Inventor(s): John Horan et al.
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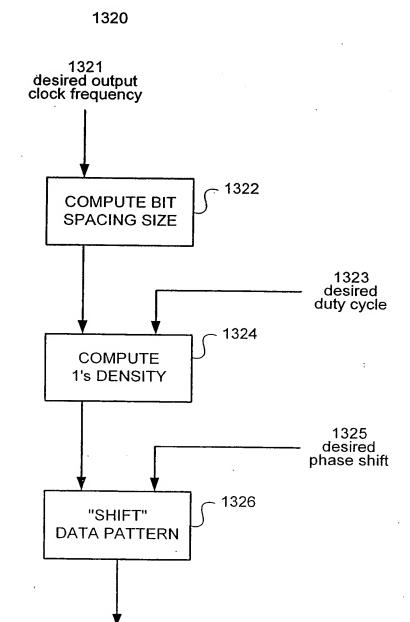


FIG. 13

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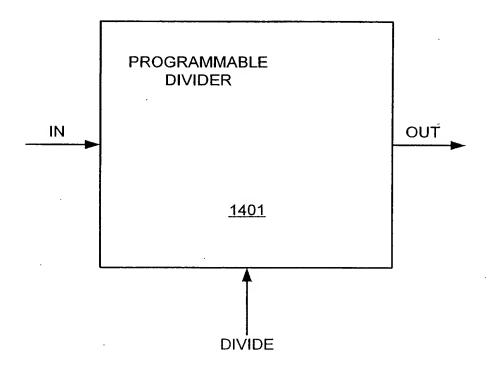


FIG. 14

Title: Method And Apparatus For Automatically Generating A Phase Lock Loop (PLL)

Generating A Phase Lock Loop (P Inventor(s): John Horan et al. Atty. Docket No.: 24198-08940

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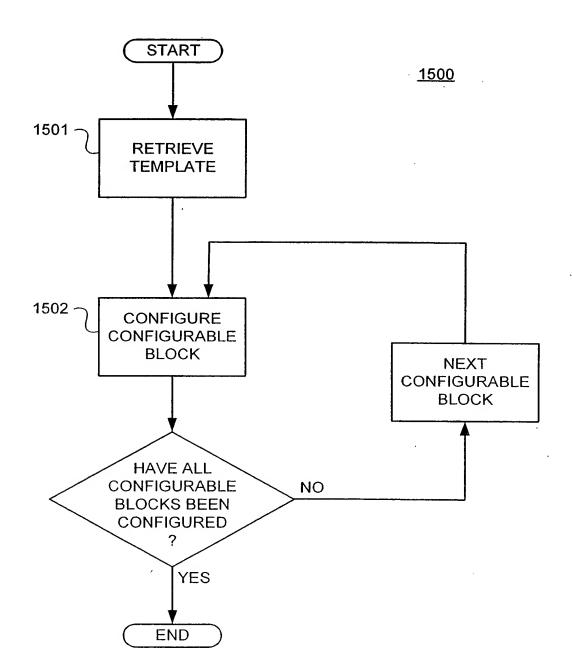


FIG. 15

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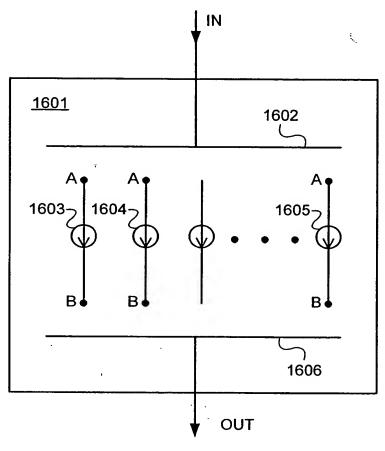


FIG. 16A

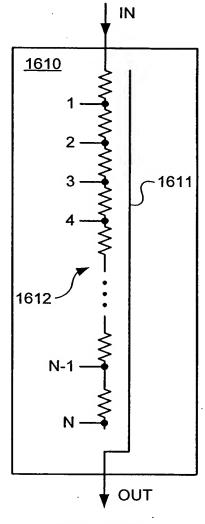


FIG. 16B